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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office
Le Président de l'Office européen des brevets
p.o.

R C van Dijk



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STMicroelectronics S.r.l.
Via C. Olivetti, 2
20041 Agrate Brianza (Milano)
ITALIE

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
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If no title is shown please refer to the description.
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Switching voltage regulator

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"Switching voltage regulator."

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DESCRIPTION

The present invention refers to a switching voltage regulator.

5 It is usually known the use of control circuits in switching static regulators employed in power suppliers wherein particular features on the precision of the regulation are requested, as in the power supply circuits of the high performance modern microprocessors. Particularly such power suppliers must provide higher and higher currents and lower and lower
10 voltages.

Switching regulators are used to perform said power suppliers. Each regulator comprises at least one MOS power transistor; particularly some regulators comprise a pair of MOS transistors or several pairs of MOS transistors which are arranged in parallel to each others and which are connected with a single output terminal by means of an inductance for each transistor pair (Multi-phase converters). The output currents of said pairs of transistors are automatically balanced by means of a control operation which detects each single current by detecting the voltage drop between the drain and source terminals of the MOS transistor. This voltage drop is also employed for implementing a well precise and programmable load regulation as a function of the current provided to the load, as it is required from particular loads such as the microprocessors.
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It is however known that the MOS transistors are provided internally of a resistance between the drain and source terminals in the conduction or firing phase, known as on or conduction resistance R_{dson} , which changes with the temperature and which, for this reason, can cause variations of the voltage signal between the drain and source terminals of the MOS transistor with currents of the same value. This occurs above all in the power MOS transistors because the current flowing through the source and drain
25
30 terminals thereof is high and consequently the variation of the voltage drop

at the terminals of the MOS transistor which is due to the thermal variation of the on resistance, is also high above all in the cases wherein, for size problems, thermal dissipators or fans are not used.

Therefore the thermal variation of the on resistance (R_{dson}) of the
5 MOS may cause very high variations of the voltage regulated by the power suppliers which employ the voltage detected between the terminals of the MOS transistor for regulating the output voltage on the load to be supplied. This may bring to non-respect of some specifications of the loads such as the microprocessors.

10 A possibility to avoid the variations of the voltage detected between the terminals of the MOS transistor of the voltage regulators consists of adding and consequently using measurement elements that are substantially invariant in temperature, for example resistors known as "sense resistors". The signal measured between the terminals of the sense resistors acts in the
15 control operation of the MOS transistor for regulating suitably the output voltage of the regulator. Such resistors have thermal variations lower than the resistance R_{dson} , are very precise but the high precision thereof is compromised by the high contact resistance due to the welding thereof on the printed circuit of the regulator. Also the power dissipated by the sense
20 resistors decreases the effectiveness of all the regulator and the use thereof causes a higher cost of all the appliance.

In view of the art described, it is an object of the present invention to provide a switching voltage regulator that overcomes the aforementioned disadvantages.

25 According to present invention, this object is attained by means of a switching voltage regulator adapted for providing a regulated voltage at an output terminal, comprising at least one MOS transistor having a non-drivable terminal coupled with said output terminal and a control circuit receiving a signal that is representative of the current signal flowing in said
30 MOS transistor, characterized in that said control circuit comprises a

compensation device adapted for cancelling the thermal variation of said signal that is representative of the current signal flowing in said MOS transistor.

Again according to present invention it is possible to provide a power supply modular system as defined in claim 9.

The features and the advantages of the present invention will be made evident by the following detailed description of an embodiment thereof, illustrated as not limiting example in the annexed drawings, wherein:

Figure 1 is a simplified circuit scheme of a switching regulator according to prior art;

Figure 2 is a scheme of a circuit part of a switching regulator according to invention;

Figure 3 is a diagram of the output voltages of the circuit in Figure 1 and of the regulator comprising the circuit part in Figure 2 as functions of the temperature;

Figure 4 is a circuit scheme of a modular power supplier according to prior art;

Figure 5 is a more detailed scheme of a circuit part of a module of the power supplier in Figure 4;

Figure 6 is a scheme of a circuit part of a module according to the present invention;

Figure 7 is a diagram of the average current of the power supplier in Figure 5 and of a modular power supplier employing the circuit part in Figure 6 in each module as functions of the temperature.

Referring to Figure 1 a switching regulator according to prior art is shown; said regulator comprises two MOS power transistors M1 and M2 where the source terminal of the transistor M1 is in common with the drain terminal of the transistor M2 and it is connected with an inductance L the other terminal of which is the output terminal of the regulator. The drain terminal of the transistor M1 is connected with an input voltage Vin while

the source terminal of the transistor M2 is connected to ground. The gate terminals of the transistors M1 and M2 (which may constitute even the electric equivalent of more MOS transistors connected with each others in parallel) are driven by means of a control circuitry 1. The transistors M1 and
5 M2 may be discrete components or may be integrated in the same chip with the control circuitry 1. The current flowing between the drain and source terminals of the transistor M2 is detected by means of a detecting device 2 that preferably comprises an amplifier able to convert the voltage drop between the terminals of the transistor M2 into a proportional current signal Ifb. The detected current Ifb is in input at the inverting terminal of an error operational amplifier 3 having the non-inverting terminal connected with a reference voltage Vprog (for example of about 1.5 V) and the output terminal connected with an impedance Z the other terminal of which is connected with the inverting terminal of the amplifier 3. The detected
10 current Ifb is brought to the output terminal of the regulator by means of a resistor Rfb arranged between the inverting terminal of the amplifier 3 and the output terminal of the regulator. In accordance with the variations of the current required from the load the current Ifb changes proportionally by causing a well precise and desired variation of the regulated voltage. The
15 variation of the on resistance Rdson2 of the MOS transistor M2 in a way depending on the temperature determines however an undesired variation of the provided current Ifb that in turn determines an undesired variation of the output voltage Vout of the regulator. In fact it occurs that $Vout = Vprog - Rfb * Ifb$ wherein the current Ifb is given by $Ifb = Iout * Rdson2 / K$ where K is a
20 proportionality constant that is function of the current detecting device 2 and Iout is the current flowing between the drain and source terminals of the transistor M2. It occurs $Vout = Vprog - Rfb * \frac{Rdson2}{K} * Iout$.
25 For avoiding variations of the regulated voltage Vout, the temperature coefficient of the term $Rfb * Rdson2 / K$ must be also cancelled and this is possible by using a thermal compensation device 9. Said device 9, shown in
30

Figure 2, comprises preferably an element 10 having a dependence on the temperature with a negative coefficient, as shown in Figure 2; in such way the total temperature coefficient may be minimized or even cancelled. A device comprising for example a series of two resistors R1 and R2 may be introduced in the place of the resistor Rfb; said element 10 is set in parallel to the resistor R2. Said element 10 is preferably constituted by a resistor NTC but it may be constituted by a diode having a suitable interface circuitry.

The thermal compensation device 9 may be formed in another way, for example using a MOS transistor and a suitable circuitry or even any bipolar transistor or JFET which is connected always with a suitable circuitry. Any component sensitive to the temperature may be used with a suitable interface circuitry for compensating the variation of the Rdson of the MOS transistor M2. The advantage of using MOS transistors or diodes as element 10 is due to integrability thereof directly on chip of the power transistor at the terminals of which the detection is effectuated.

In Figure 3 the waveforms of the output voltages Vout1 (with a sketch line) and Vout2 (with a continuous line) as functions of the temperature are shown which respectively regard the voltage regulator in Figure 1 and the regulator employing the thermal compensation device according to invention. The voltages Vout1 and Vout2 are valued in the different cases wherein the value of the current Iout (in Figure 3 Iout=I) is 0 A, 10 A, 20 A, 30 A, 40 A, 50 A; using I=0 A the voltages Vout1 and Vout2 are equal. The used element NTC is a PANASONIC ERTJ1VT102H. From the diagram it is evident that the voltage Vout is substantially constant changing the temperature.

In Figure 4 a modular power supply is shown according to prior art. Said power supply comprises various modules 100 arranged in parallel to each other and which have a same input voltage Vi. Each module 100 comprises a supply 101, a MOS transistor 102 (which may constitute even

the electric equivalent of more MOS transistors connected with each other in parallel) connected in series with the power supply 101 and with the output terminal OUT of the modular power supply and a control circuit 103. The last detects the current I102 flowing through the transistor 102 and provides
5 an input signal to the supply 101 and a signal Vbus which finds on the bus 200 (current-sharing BUS) that is common to all the modules 100 and on which the information relating to the average current brought by the modular power supply is formed wherein it is meant by average current the mean of the currents brought by each module 100. Each module 100 compares the
10 own current with the average current and amends its operation to cancel such difference.

The control device 103, more shown in Figure 5, comprises an amplifier 104 adapted for detecting the current I102 flowing through the MOS transistor 102, a buffer 105 having an input voltage signal at the inverting terminal which is given by the current signal Iout1 in output from the amplifier 104 which is multiplied by a resistor Rcg_a and the output signal thereof is in input to a current-sharing BUS 200. The control device 103 comprises an error amplifier 106 having in input the same voltage signal given by the current signal Iout1 in output from the amplifier 104 which is multiplied by a resistor Rcg_a and a signal storing the information relating to the average current deriving from the current-sharing BUS 200. The output signal of the amplifier 106 is in input to the power supply 101 and it is a correction signal; said signal allows to correct the operation of each power supply 101 in such a way to make equal the current I102 of each module 100
15 with the average current brought totally by the modular power supply.
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25

The voltage Vbus for each single module 100 is given by:

$$V_{bus} = R_{cg\alpha} * \frac{R_{dson}}{k_1} * I_{out1}$$

For avoiding variation of the voltage Vbus with respect to the temperature the temperature coefficient of the term Rcg_a*R_{dson}/K₁ must be also cancelled; this is possible by using a thermal compensation device 9
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already described. Said device 9 comprises preferably an element 10 having a dependence on the temperature with a negative coefficient, as shown in Figure 6; in such way the total temperature coefficient may be cancelled. A device comprising for example a series of two resistors R1 and R2 may be introduced in the place of the resistor R_{cga}; said element 10 is set in parallel to the resistor R2. Said element 10 is preferably constituted by a resistor NTC but it may be constituted by a diode having a suitable interface circuitry.

The thermal compensation device 9 may be formed in another way, for example using a MOS transistor and a suitable circuitry or even any bipolar transistor or JFET which is connected always with a suitable circuitry. Any component sensitive to the temperature may be used with a suitable interface circuitry for compensating the variation of the Rdson of the MOS transistor 102.

In Figure 7 the waveforms of the output voltages Vbus1 (with a sketch line) and Vbus2 (with a continuous line) on the bus 200 as function of the temperature are shown which respectively regard the power supply in Figure 4 and the power supply employing the thermal compensation device according to invention. The voltages Vbus1 and Vbus2 are valued in the different cases wherein the value of the current I102 (in Figure 7 I102=I) is 10 A, 25 A, 40 A. The element NTC used is a PANASONIC ERTJ1VT102H. From the diagram it is evident that the voltage Vbus2 is substantially constant changing the temperature.

CLAIMS

1. Switching voltage regulator adapted for providing a regulated voltage (Vout) at an output terminal (OUT), comprising at least one MOS transistor (M2, 102) having a non-drivable terminal coupled with said output terminal (OUT) and a control circuit (1-3, 103) receiving a signal (Ifb, Iout1) that is representative of the current signal flowing in said MOS transistor (M2, 102), characterized in that said control circuit (1-3, 103) comprises a compensation device (9) adapted for cancelling the thermal variation of said signal (Ifb, Iout1) that is representative of the current signal flowing in said MOS transistor (M2, 102).
5
2. Regulator according to claim 1, characterized in that said compensation device (9) comprises an element (10) having a negative temperature coefficient.
10
3. Regulator according to claim 2, characterized in that said compensation device (9) comprises a first (R1) and a second (R2) resistors connected in series, said negative temperature coefficient element (10) being arranged in parallel to said first (R1) or second (R2) resistor.
15
4. Regulator according to claim 3, characterized in that said negative temperature coefficient element (10) is a NTC resistor.
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5. Regulator according to claim 3, characterized in that said negative temperature coefficient element (10) is a diode.
25
6. Regulator according to claim 1, characterized in that said MOS transistor (M2) is a MOS power transistor having a non-drivable terminal coupled with an input voltage (Vin), and in that said control circuit (1-3) comprises a driving device (1) of said MOS power transistor (M2) which is coupled with its gate terminal, a first device (2) which is adapted for detecting the current flowing through said MOS power transistor (M2) and which is able to provide at an output terminal said signal (Ifb) that is representative of the current signal flowing in said MOS transistor (M2), a second device (3) which is coupled with said first device (2) and which is
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able to compare said signal (I_{fb}) in output from said first device (2) with a reference signal (V_{prog}) and which is able to provide a correction signal to the driving device (1), said compensation device (9) being coupled with the output terminal of the first device (2) and with the output terminal of said voltage regulator.

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7. Regulator according to claim 6, characterized in that said second device (3) is an error amplifier having the input inverting terminal connected with the output terminal of the first device (2) and with the compensation device (9)

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8. Regulator according to claim 7, characterized in that said first device (2) comprises a transconductance amplifier.

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9. Power supply modular system comprising at least two single switching regulators (100) arranged in parallel to each other, each of said regulators (100) being adapted for providing a regulated voltage (V_{out}) at an output terminal (OUT) and comprising at least one MOS transistor (102) having a non-drivable terminal coupled with said output terminal (OUT) and a control circuit (103) receiving a signal (I_{out1}) that is representative of the current signal flowing in said MOS transistor (102), characterized in that said control circuit (103) comprises a compensation device (9) adapted for cancelling the thermal variation of said signal (I_{out1}) that is representative of the current signal flowing in said MOS transistor (102).

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10. System according to claim 9, characterized in that said compensation device (9) comprises an element (10) having a negative temperature coefficient.

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11. System according to claim 10, characterized in that said compensation device (9) comprises a first (R1) and a second (R2) resistors connected in series, said negative temperature coefficient element (10) being arranged in parallel to said first (R1) or second (R2) resistor.

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12. System according to claim 10, characterized in that said negative temperature coefficient element (10) is a NTC resistor.

13. System according to claim 11, characterized in that said negative temperature coefficient element (10) is a diode.

14. System according to claim 9, characterized in that said at the least two switching regulators (100) have a common input voltage (V_i), each one of said regulators (100) comprising supply means (101) coupled with said MOS transistor (102) connected in turn with an output terminal (OUT) of said modular system, and in that said control circuit (103) is coupled with the MOS transistor (102), with said supply means (101) and with a bus (200) which is common to all said at the least two switching regulators (100) and which is adapted for bringing the information of the average current brought totally by said system, said control circuit (103) comprising a first device (2) which is adapted for detecting said current flowing between the drain and source terminals of said MOS transistor (102) and which is able to provide at an output terminal said signal (I_{out1}) that is representative of the said current (I_{102}), said compensation device being coupled with said first device (104) in order to provide in output a compensated signal, said control circuit (103) comprising first means (105) able to provide a signal (V_{bus}) representative of the compensated signal to said bus (200) and second means (106) able to provide a correction signal to said supply means (101) in order 10 the current signal of each regulator to make equal to said average current.

15. System according to claim 14, characterized in that said first means (105) comprises a buffer having in input said compensated signal and said second means (106) comprises an error amplifier having said compensated signal at the inverting terminal and a signal representative of said average current coming from said bus at the non-inverting terminal.

"Switching voltage regulator."

* * * * *

ABSTRACT

A switching voltage regulator adapted for providing a regulated voltage (Vout) at an output terminal (OUT) is described which comprises at least one MOS transistor (M2, 102) having a non-drivable terminal coupled with said output terminal (OUT) and a control circuit (1-3, 103) receiving a signal (Ifb, Iout1) that is representative of the current signal flowing in said MOS transistor (M2, 102). The control circuit (1-3, 103) comprises a compensation device (9) adapted for cancelling the thermal variation of said signal (Ifb, Iout1) that is representative of the current signal flowing in said MOS transistor (M2, 102). (Figure 2)

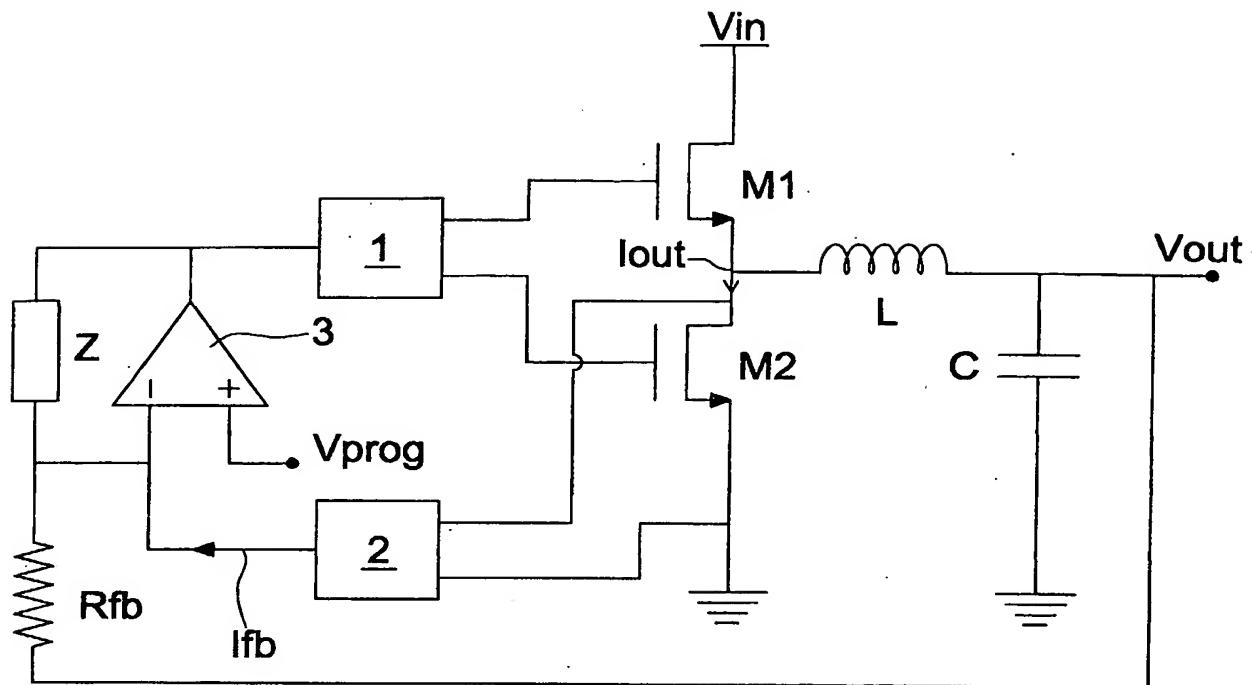


Fig.1

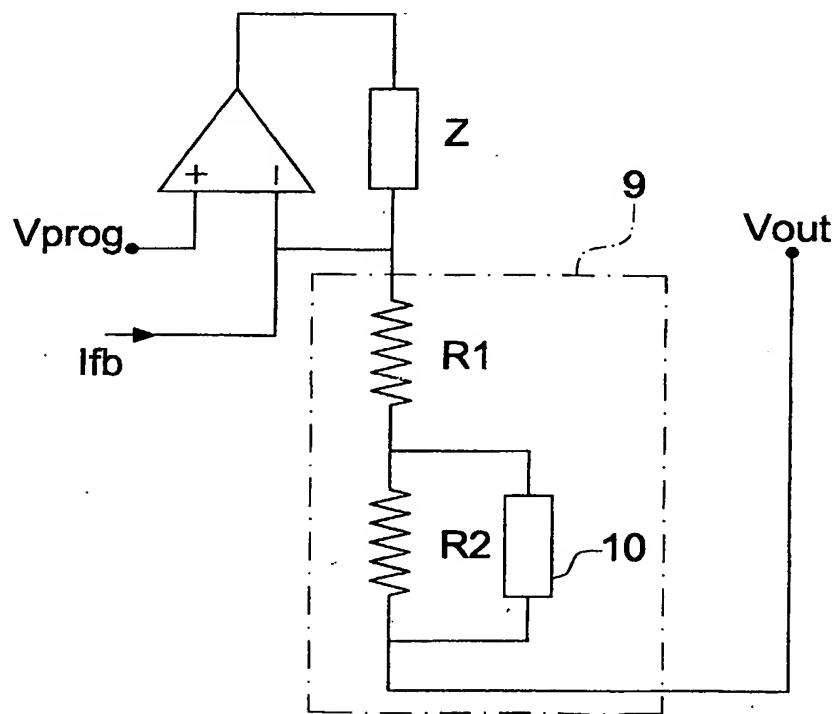


Fig.2

2/3

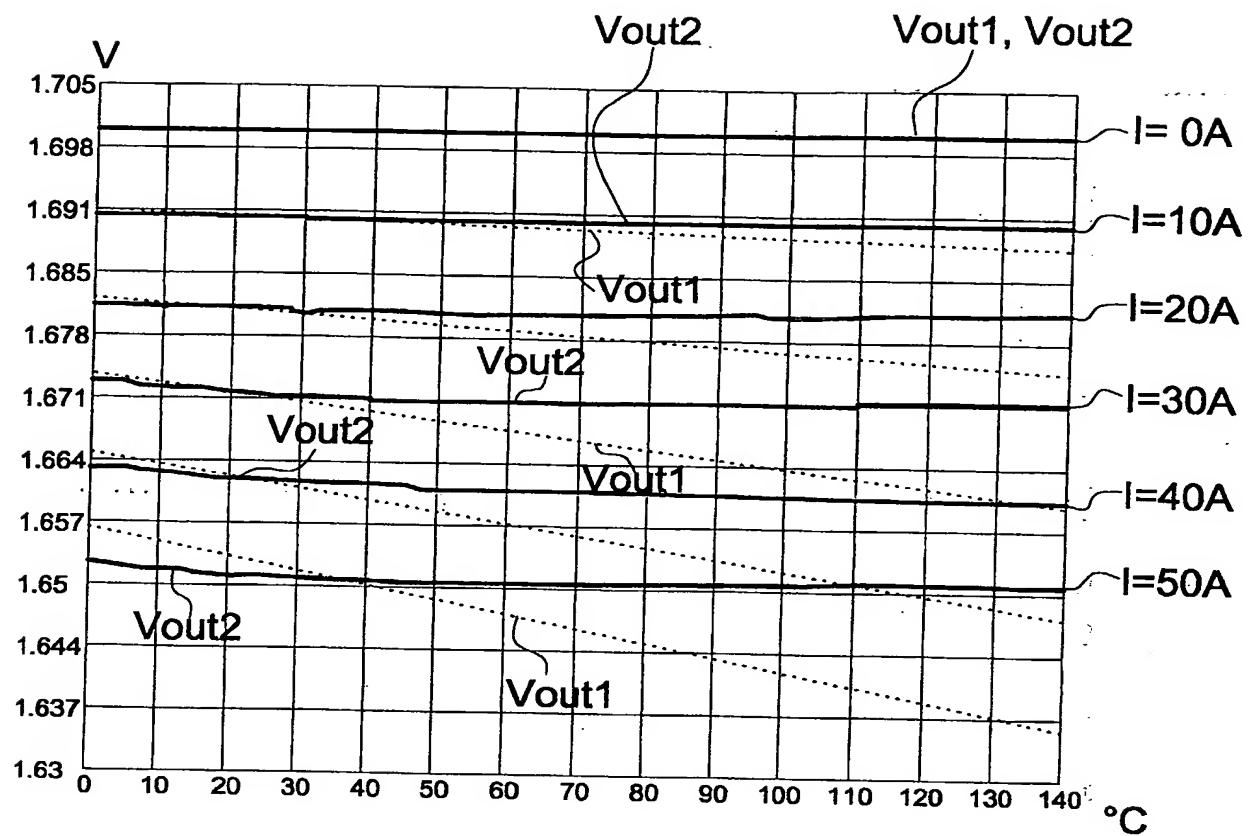


Fig.3

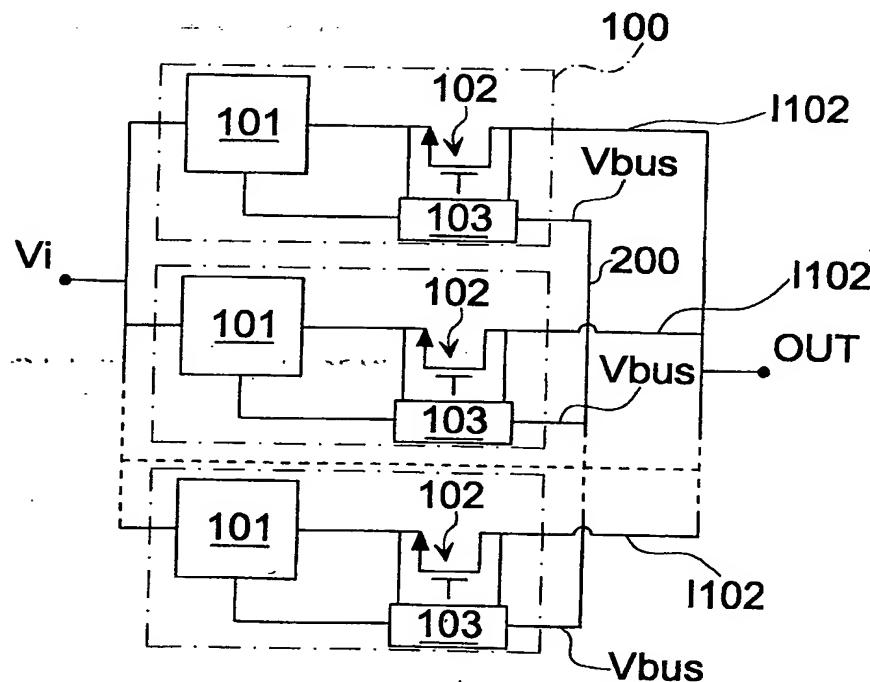


Fig.4

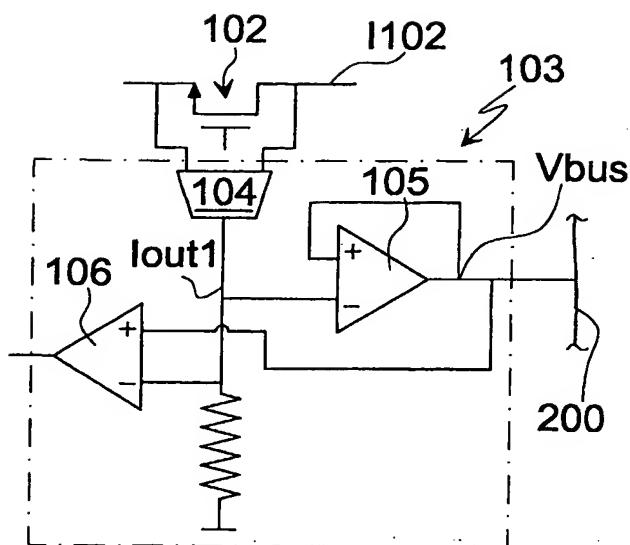


Fig.5

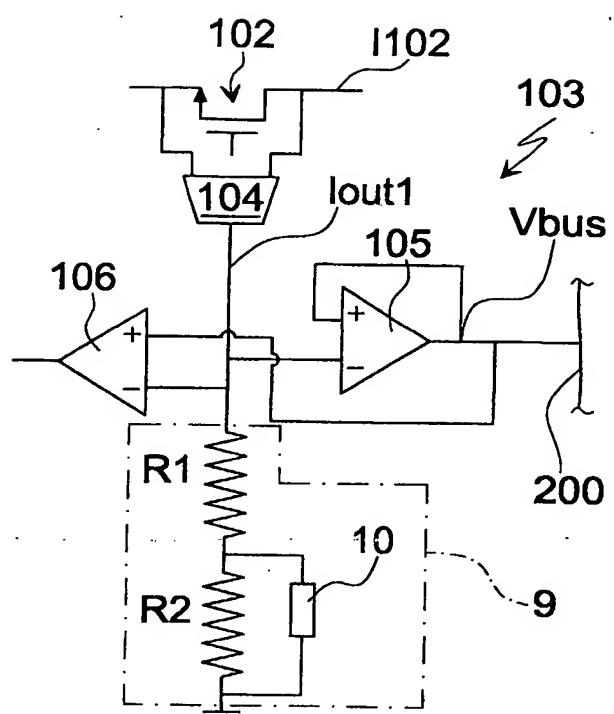


Fig.6

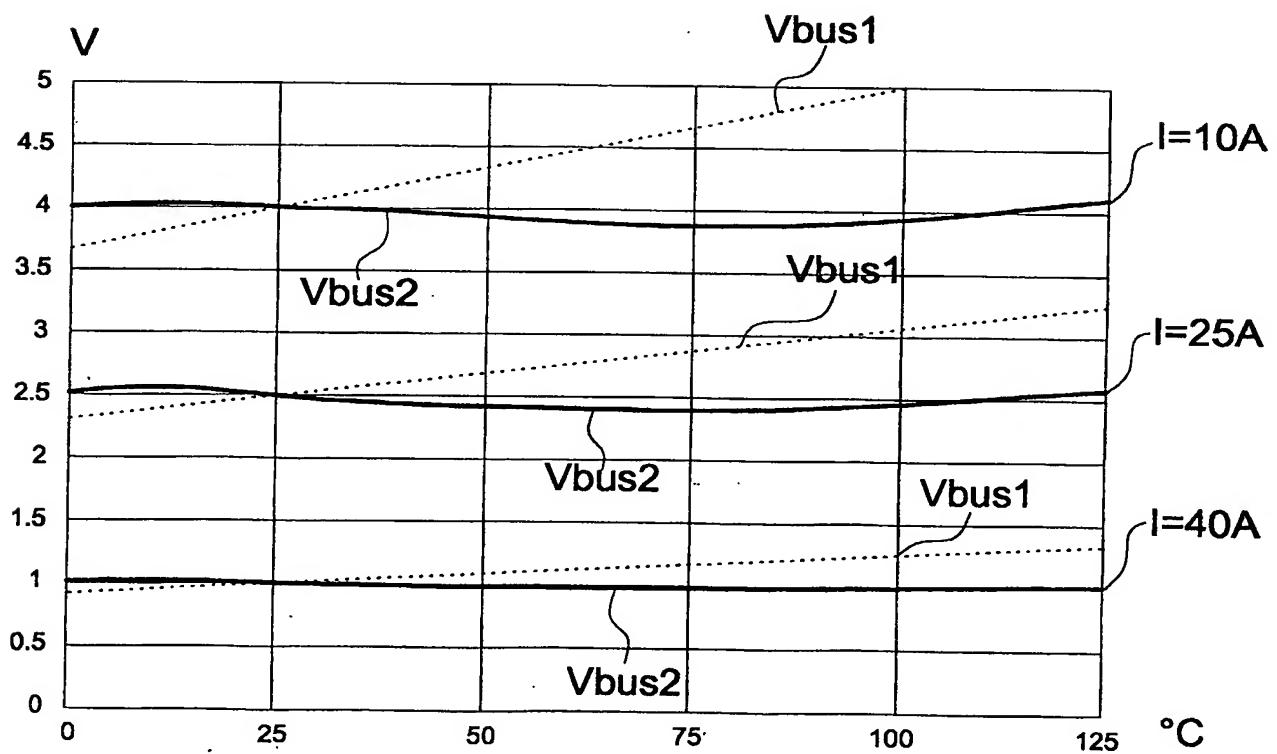


Fig.7

